What is claimed is:

1. A test device for detecting alignment of deep trench capacitors and word lines in DRAM devices, wherein the test device is disposed in a scribe line region of a wafer, the scribe line region having a plurality of pairs of memory cells, each having two deep trench capacitors deposed at two ends of an active area, two word lines disposed above the active area, and a bit line contact disposed between the two word lines and electrically coupled to the active area, the test device comprising:

parallel first and second bar-type deep trenches capacitors disposed in the scribe line region; wherein the first and second bar-type deep trenches capacitors extend to the first and second pairs of memory cells adjacent to the first active area respectively, and are electrically coupled to bit line contacts of the first and second pairs of memory cells respectively;

a first transistor having a source coupled to the first bar-type deep trench capacitor;

a second transistor having a source coupled to the second bar-type deep trench capacitor; and

a first bit line contact electrically coupled to drains of the first and second transistors.

2. The test device as claimed in claim 1, wherein two word lines are disposed on two sides of the first bit

line contact respectively, as gates of the first and the second transistors respectively.

3. The test device as claimed in claim 2, wherein a first resistance between the first bit line contact and the bit line contact of the first pair of memory cells is detected by turning on the first transistor, and a second resistance between the second bit line contact and the bit line contact of the second pair of memory cells is detected by turning on the second transistor.

4. A semiconductor device with a test device, comprising:

a substrate having a least one scribe line region and a memory region, wherein the scribe line region and the memory region both have a plurality of pairs of memory cells, each including:

an active area;

two deep trench capacitors deposed at two ends of the active area;

two word lines disposed above the active area; and

a bit line contact disposed between the two word lines and electrically coupled to the active area; and

a test device disposed in the scribe line region, comprising:

parallel first and second bar-type deep trenches capacitors disposed in the scribe line region; wherein the first and second

bar-type deep trenches capacitors extend to the first and second pairs of memory cells adjacent to the first active area respectively, and electrically coupled to bit line contacts of the first and second pairs of memory cells respectively;

a first transistor having a source coupled to the first bar-type deep trench capacitor;

a second transistor having a source coupled to the second bar-type deep trench capacitor; and

a first bit line contact electrically coupled to drains of the first and second transistors.

5. The semiconductor device as claimed in claim 4, wherein two word lines are disposed on two sides of the first bit line contact respectively, as gates of the first and the second transistors respectively.

6. The semiconductor device as claimed in claim 4, wherein a first resistance between the first bit line contact and the bit line contact of the first pair of memory cells is detected by turning on the first transistor, and a second resistance between the second bit line contact and the bit line contact of the second pair of memory cells is detected by turning on the second transistor.

7. A method for detecting alignment of deep trench capacitors and word lines in DRAM devices, comprising:

providing a wafer with at least one scribe line region and at least one memory region;

forming a plurality of pairs of memory cells in the memory region and at least one test device in the scribe line simultaneously, wherein each pair of memory cells includes an active area, two deep trench capacitors deposed at two ends of the active area, two word lines disposed above the active area, and a bit line contact disposed between the two word lines and electrically coupled to the active area, the test device including:

parallel first and second bar-type deep trenches capacitors disposed in the scribe line region; wherein the first and second bar-type deep trenches capacitors extend to the first and second pairs of memory cells adjacent to the first active area respectively, and electrically coupled to bit line contacts of the first and second pairs of memory cells respectively;

a first transistor having a source coupled to the first bar-type deep trench capacitor;

a second transistor having a source coupled to the second bar-type deep trench capacitor; and

a first bit line contact electrically coupled to drains of the first and second transistors;

measuring a first resistance between the first bit line contact and the bit line contact of the first pair of memory cells and a second resistance between the second bit line contact and the bit line contact of the second pair of memory cell; and

determining alignment of the deep trench capacitors and word lines in the memory regions according to alignment of the first and second resistance.

8. The method as claimed in Claim 7, wherein two word lines are disposed on two sides of the first bit line contact respectively, as gates of the first and the second transistors respectively.

9. The method as claimed in Claim 8, further comprising:

determining alignment of the first and second bar-type deep trenches capacitors and two word lines of the test device according to the first resistance and the second resistance; and

determining alignment of the deep trench capacitors and word lines in the memory regions according to alignment of the first and second bar-type deep trenches capacitors and two word lines of the test device.